

REMARKS

The examiner rejected claims 1-23 under 35 U.S.C. 102(b) as being anticipated by Chang et al US Patent 5,634,015.

The examiner, the undersigned, and Ms. Tonya Drake, acting under the undersigned's direction had a telephonic interview on December 3, 2004. Discussed was claim 1. Applicant has amended claims 1, 9, and 16 as discussed during the telephone interview to add the limitation that the queue descriptors that are stored in the memory, but not included in the determined subset, are not stored in the cache. Chang does not disclose or suggest that the determined subset of queue descriptors stored in the cache includes less than all of the queue descriptors stored in the memory with the queue descriptors that are stored in the memory, but not included in the determined subset, not being stored in the cache; as in the applicant's claim 1. Therefore, Claims 1-23 as amended are distinct over Chang.

Chang stores system packets in a packet memory. Due to the length of a particular packet, the packet may be partitioned into multiple buffers within the memory. Two memories (GAM 18 and GAM local memory 30) are used to track the location of the packet data in the memory. The GAM 18 is used to track the packets and "has one packet table entry (PTE) in its local memory for each existing packet in the PM" (emphasis added, col. 17, lines 60-63). Since the packet may have been divided into multiple buffers, the GAM local memory 30 tracks the multiple buffers for each packet. "For each buffer in the packet memory (PM) there is one corresponding buffer table entry in the GAM local memory 30" (emphasis added, col. 17, lines 24-26).

Since Chang stores an entry corresponding to each buffer in the GAM local memory 30, the GAM local memory does not store queue descriptors each specifying a structure of a respective queue, the queue including a linked list of elements and the queue descriptor including a head pointer, a tail pointer, and a count as in the applicant's claim 1. As described above, Chang also includes a GAM memory 18 that has an entry for each existing packet in the PM. Since the GAM memory 18 includes an entry for each packet, it is not equivalent to the applicant's cache which stores a determined subset of queue descriptors that includes less than all of the queue descriptors that are stored in the memory where the queue descriptors stored in the memory, but not included in the determined subset, are not stored in the cache. Therefore, Claims 1-23 as amended are distinct over Chang.

For at least the same reasons, applicant submits claim 1 should be allowed, applicant submits that dependent claims 2-8 should be allowed.

Claim 9 distinguishes by reciting a memory controller logic that includes a cache to store a subset of the queue descriptors in the memory, the subset determined based on which of the queue descriptors stored in the memory were most recently accessed, and the determined subset of queue descriptors stored in the cache including less than all of the queue descriptors stored in the memory with the queue descriptors that are stored in the memory, but not included in the determined subset, not being stored in the cache. Thus, based on these limitations claim 9 is patentable for reasons similar to claim 1.

For at least the same reasons, applicant submits claim 9 should be allowed, applicant submits that dependent claims 10-15 should be allowed.

Applicant : Gilbert Wolrich et al.
Serial No. : 10/041,678
Filed : January 7, 2002
Page : 10 of 10

Attorney's Docket No.: 10559-610001 / P12849

Claim 16 includes instructions causing a computer to store the determined subset of queue descriptors in a cache in a processor's memory controller logic, the determined subset of queue descriptors stored in the cache including less than all of the queue descriptors stored in the memory with the queue descriptors that are stored in the memory, but not included in the determined subset, not being stored in the cache. Thus, based on these limitations claim 16 is patentable for reasons similar to claim 1.

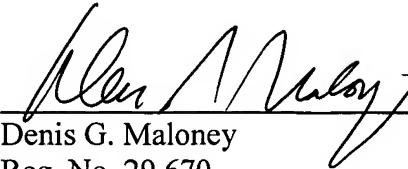
For at least the same reasons, applicant submits claim 16 should be allowed, applicant submits that dependent claims 17-23 should be allowed.

The fact that the applicant has addressed certain comments of the examiner does not mean that the applicant concedes any other positions of the examiner. The fact that the applicant has asserted certain grounds for the patentability of a claim does not mean that there are not other good grounds for patentability of that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, referencing Attorney Docket No. 10559-610001.

Respectfully submitted,

Date: 12/08/07



Denis G. Maloney
Reg. No. 29,670

Fish & Richardson P.C.
225 Franklin Street
Boston, MA 02110-2804
Telephone: (617) 542-5070
Facsimile: (617) 542-8906